DATA SHEET

SAA7274
Audio Digital Input Circuit (ADIC)

Product specification
File under Integrated Circuits, IC01

July 1991

Philips
Semiconductors

PHILIPS

Audio Digital Input Circuit (ADIC) SAA7274

GENERAL DESCRIPTION

The SAA7274 is an Audio Digital Input Circuit (ADIC) which converts digital audio signals in accordance with the IEC/EBU standards, IEC tech. com. No. 84, secr. 50, Jan. 1987 into an equivalent binary value of data and control bits. The output function of this device is to convert the equivalent binary value of data bits (for each channel) into a serial digital audio signal which conforms to the I^2S format.

Features

- I^2S bus output
- Biphase audio signal (Satellite radio, compact disc and DAT)

QUICK REFERENCE DATA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply						
Supply voltage range	except IBIFA	V_{DD}	4.5	–	5.5	V
Inputs						
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Input voltage LOW		V_{IL}	0	–	0.3 V_{DD}	V
Input current	V_I = 0 V	$-I_I$	–	–	1	µA
	V_I = 5.5 V	I_I	–	–	1	µA
Input capacitance		C_I	–	4	6	pF
Outputs						
Output voltage HIGH		V_{OH}	V_{DD}–0.5	–	–	V
Output voltage LOW		V_{OL}	–	–	0.4	V
Operating ambient temperature range		T_{amb}	–40	–	+70	°C

PACKAGE OUTLINES

SAA7274P: 24-lead DIL; plastic (SOT101A); SOT101-1; 1996 September 05.

SAA7274T: 24-lead mini-pack; plastic (SO24; SOT137A); SOT137-1; 1996 September 05.

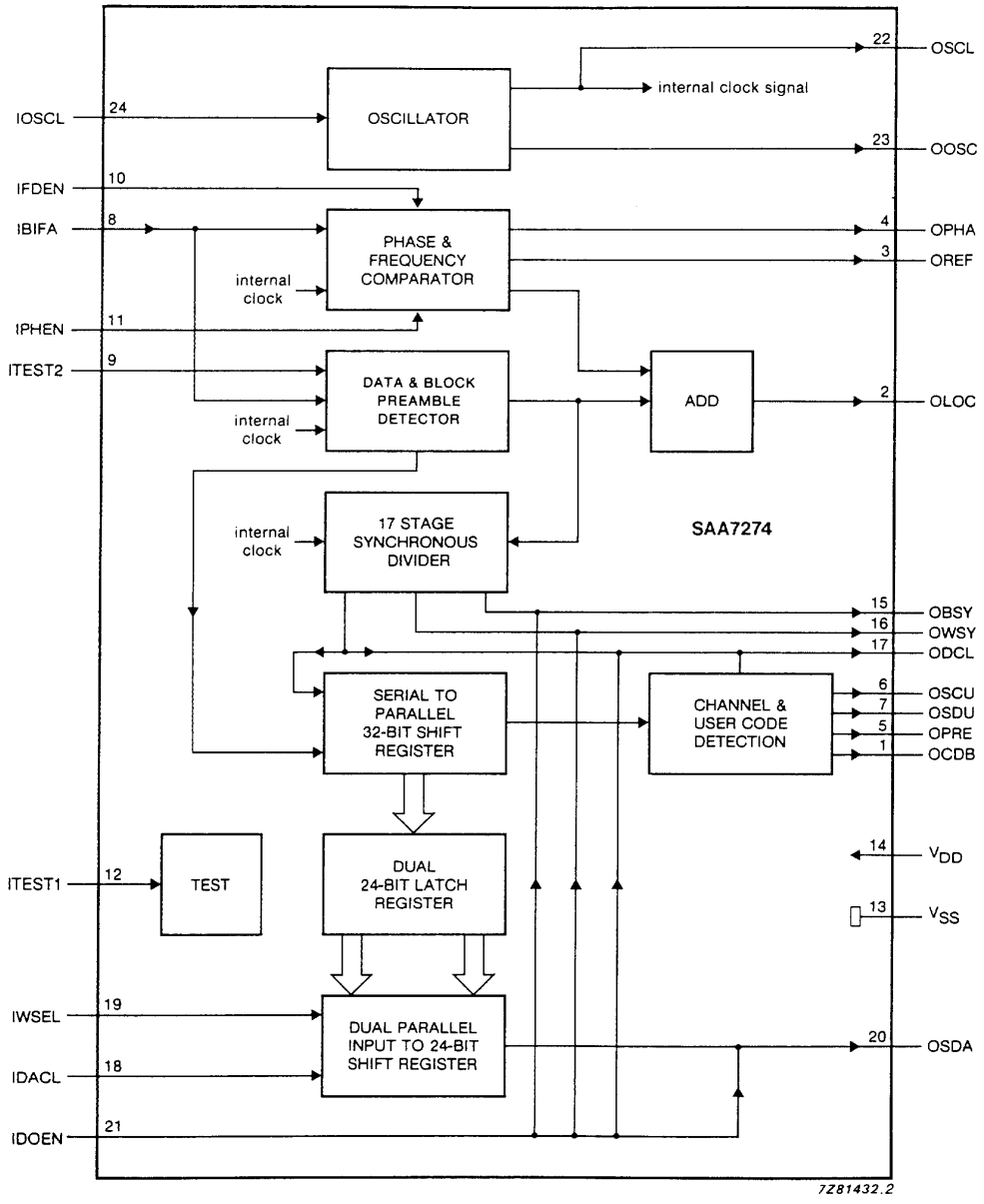


Fig.1 Block diagram.

PINNING

Power supply	
V_{DD}	positive supply voltage (5 V)
V_{SS}	ground (0 V)
Inputs (CMOS protection)	
IBIFA	biphase input signal (min. 1 MHz; max. 3.1 MHz)
IFDEN	frequency detector enable
IPHEN	phase-locked loop edge selector
ITEST1	test input enable
ITEST2	test input enable
IDACL	data clock input signal (max. 5 MHz)
IWSEL	word select input signal (max. 50 kHz)
IDOEN	output enable
IOSCL	clock oscillator input (min. 8 MHz; max. 12.5 MHz)
Outputs (CMOS push-pull)	
OCDB	control data bits (max. 400 kHz)
OLOC	out-of-lock signal
OREF	phase reference signal (max. 6.2 MHz)
OPHA	phase output signal (max. 6.2 MHz)
OPRE	pre-emphasis level
OSCU	user clock/copy-bit signal (max. 3.1 MHz)
OSDU	user data/pre-emphasis (max. 3.1 MHz)
OSCL	system clock output (min. 8 MHz; max. 12.5 MHz)
OOSC	clock oscillator output (min. 8 MHz; max. 12.5 MHz)
Outputs (3-state push-pull)	
OBSY	block synchronization output signal (1/49152 system clock)
OWSY	word clock output signal (1/256 system clock)
ODCL	data clock output signal (1/4 system clock)
OSDA	data output signal (max. 2.5 MHz)

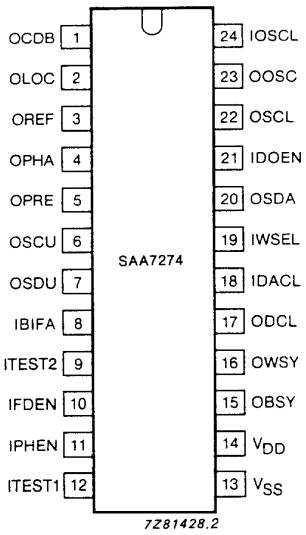


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Main function

The biphase input signal must conform to the IEC/EBU standards, IEC tech. com. No. 84, secr. 50, Jan. 1987 format, as well as satisfying the following conditions:

- number of channels: 2
- transmission code: biphase mark
- synchronization method: biphase violation
- number of data bits: 24, starting with the LSB
- number of control bits: 4
- preamble values:

Table 1 Preamble values

preceding cell	0	1
block preamble	11101000	00010111

The main function performs the following tasks:

- Provides the output function with the equivalent binary value of the data bits separately for each of the two channels. These values are available until new information is received.
- Generates an out-of-lock output signal (OLOC) which is HIGH when the frequency of the biphase input signal is equal to 1/4 of the system clock frequency and when the block preambles are detected in the biphase input signal.
- If the biphase input signal is not present after 32 clock pulses and also whenever the biphase input signal and IOSCL/4 drift away from each other by more than 32 clock pulses, then the output OSCU is forced HIGH and output OSDU, OPRE, OLOC, OCDB and OSDA are forced LOW.
- Generates a data clock output signal (ODCL) with a frequency of 1/4 of the system clock. When a block preamble is detected in the biphase input signal ODCL is synchronized to a LOW value.
- Generates a word clock output signal (OWSY) with a frequency of 1/256 of the system clock. When a block preamble is detected in the biphase input signal OWSY is synchronized to a LOW value.
- Generates a block synchronization output signal (OBSY). This signal is HIGH during 4 system clock periods and has a frequency of 1/49152 of the system clock. The signal is synchronized with the block preambles of the biphase input signal.
- Generates a phase output signal (OPHA) and a phase reference signal (OREF). If the frequency of the biphase input signal (IBIFA) equals 1/4 of the system clock frequency ($f_{IOSCL}/4$) then the IC generates OPHA and OREF as shown in Fig.3.
  If the frequency of the biphase input signal (IBIFA) is greater or less than 1/4 of the system clock frequency then the IC generates OPHA and OREF as shown in Fig.4.

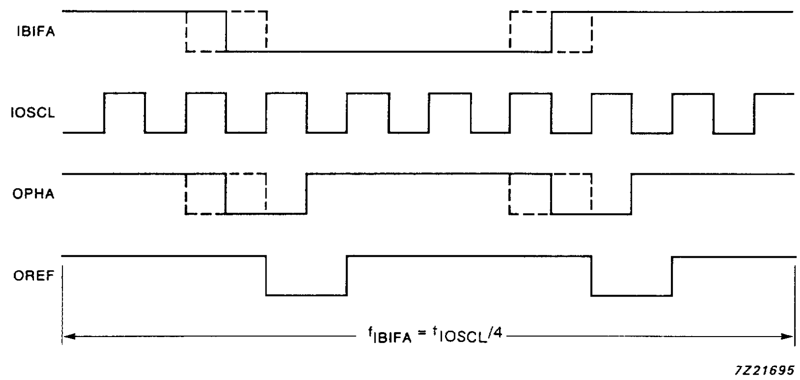


Fig.3 Generation of phase output signal (OPHA) and phase reference signal (OREF); $f_{IBIFA} = f_{IOSCL}/4$.

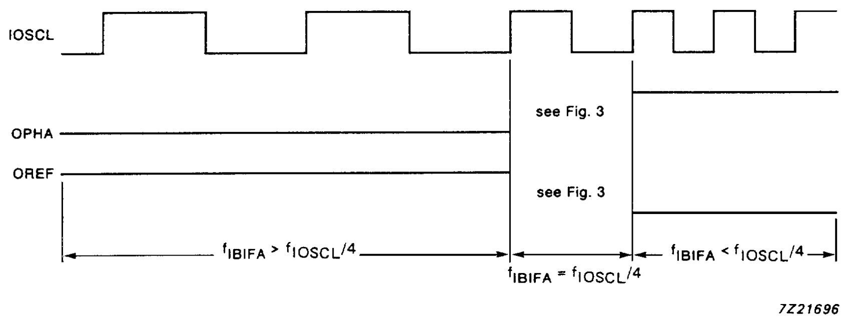


Fig.4 Generation of phase output signal (OPHA) and phase reference signal (OREF); $f_{IBIFA} = f_{IOSCL}/4$.

Output function

The output function performs the following tasks:

- Provides the data output (OSDA) with the data bits from each channel in the following order:

Table 2 Order of databits

MSB	LSB	0	0	0	0	0	0	0	0

- Outputs the data of the right and left channel. When word select input signal (IWSEL) is HIGH the data of the right channel is output and when LOW the data of the left channel is output.
- Delivers serial data to the OSDA output, if IDOEN = HIGH. This occurs on each negative transition of the data clock input signal (IDACL). Following a status change at the word select input (IWSEL), the data (MSB first) is output on the first negative transition of IDACL. If the number of clock pulses in a word exceeds 24, then the following bits will be internally set to zero.

- Generates the following subcodes:

Table 3 Subcode generation

series 1,	0	0	U1	T1	S1	R1	Q1	1	0	0
series 2,	CRC	0	V1	U1	T1	S1	R1	Q1	1	0
series 3,	0	0	W1	V1	U1	T1	S1	R1	Q1	1
and after receiving the next user byte:										
series 4,	0	0	W2	V2	U2	T2	S2	R2	Q2	1 etc.

- If the value of the category bits, bits 9 to 16 of the input signal, = 10000000 (compact disc format) and the value of the mode bits, bits 7 and 8, = 00, the user data output (OSDU) will deliver the bits of the subcode following the specified lay-out (above). The subcode starts only after receipt of at least 16 zero bits. Simultaneously a user clock signal (OSCU) consisting of 10 clock pulses is present. The output signal starts when a subcode is completed and is clocked on the negative transition of OSCU. The first data word of each subcode frame is output 3 times in succession with the data pattern shifted each time as outlined for series 1 through series 3 in the layout given above. The CRC performs a check on the 96 Q bits of the preceding subcode. If CRC is correct then the CRC bit = 1.
- Channel status:

Table 4 Channel status

1	2	3(1)	4(2)	5	6	7	8	9	10	11	12	13	14	15	16	.	.	.
control		.	.	res	.	mode		category										

Notes

1. copy permitted.
2. pre-emphasis.

If the value of the category bits **does not** equal 10000000 (compact disc format) and the value of the mode bits equals 00 (mode 0), then:

output OSDU indicates the status of bit 4 (pre-emphasis) of the channel status and output

OSCU indicates the status of bit 3 (copy permitted) of the channel status provided the control bits conform to the 2-channel audio signal format.

- Uses the output pre-emphasis (OPRE) to indicate the status of bit 4 of the channel status for a 2-channel audio signal.
- Outputs the 4 control bits of the biphase input signal (IBIFA) represented by V, U, C and P at OCDB. The output delivers the bits in the same sequence during the next word, each bit continues for 32 clock pulses.

Additional input and output signals

The following input and output signals are available from this circuit:

- Phase output signal (OPHA) and phase reference signal (OREF) for use in a phase-locked loop (PLL). The OPHA signal is a result of the difference between the frequency and phase of the biphase input signal and the system clock. OREF signal provides the reference signal for the PLL.
- Input signal IFDEN enables the frequency detector. The frequency detection as present in the 2 signals OPHA and OREF can be enabled by making this signal LOW.
- Data clock output signal (ODCL), which has a frequency of 1/4 of the system clock frequency.
- Word clock output signal (OWSY), which has a frequency of 1/256 of the system clock frequency.
- Block synchronization output signal (OBSY), which has a frequency of 1/49152 of the system clock.
- ODCL, OWSY and OBSY will be synchronized to the block preambles in the biphase input signal IBIFA.

- Outputs ODCL, OWSY, OBSY and OSDA are enabled via a 3-state mode with a HIGH level on input IDOEN.
- IPHEN input selects dual or single edge detection of the input signal IBIFA in the phase detector. A low level selects the single-edge detection mode.
- Out-of-lock signal (OLOC). This output is continuously LOW or random HIGH/LOW if the PLL is out-of-lock, or no block preambles and present in the biphase input signal IBIFA. It is continuously HIGH if the PLL is in lock.
- User data/pre-emphasis output signal (OSDU). After receiving a category code of mode 0 from a non-compact disc source this signal outputs the pre-emphasis bit of the channel status bits in the biphase input signal. If the category code of mode 0 is from a compact disc source then the user data bits from the subcode channel including the CRC check on the 96 preceding Q bits are output.
- User clock/copy bit output signal (OSCU). After receiving a category code of mode 0 from a non-compact disc source then the copy bit of the channel status bits in the biphase input signal is output. If the category code of mode 0 is from a compact disc source then 10 clock pulses for the ‘user data’ are output.
- Pre-emphasis level output signal (OPRE), which indicates the value of the pre-emphasis bit of the channel status bits after receiving the two-channel audio format in the biphase input signal (IBIFA).
- Control data bits output signal (OCDB), which contains the 4 control bits of each word of the biphase input signal.
- The inputs ITEST1 and ITEST2 are used for device tests at the factory only, for normal operation they have to be connected to V_{SS}.

Clock oscillator

The clock oscillator of the circuit can be formed by connecting a crystal or a ceramic resonator between the oscillator input and output pins.

The circuit can also be driven by an external signal source applied to the oscillator input. The oscillator output is buffered and available at pin OSCL. The internal circuitry is driven via an inverter, which is connected to the output OSCL. This allows all the output signals (especially ODCL, OWSY and OBSY) to change their state after a pulse from OSCL, independent of the capacitive load of the OSCL pin. All output signals of the circuit are triggered on the positive transition of the OSCL signal.

Application note

If the capacitive load is higher than specified in **AC CHARACTERISTICS**, a buffer circuit can be used. A suitable device is the PC74HC126 (3-state quad buffer/line driver). The input IDOEN to the SAA7274 must be made HIGH and the original 3-state enable signal must be connected to the OE inputs of the PC74HC126 (pins 1, 4, 10 and 13). Because the capacitive load of the SAA7274 is very low, the loss of speed is limited.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Supply voltage range		V_{DD}	–0.5	7.0	V
Input voltage	note 1	V_I	–0.5	V_{DD}+0.5	V
Maximum input current		I_{IM}	–	±10	mA
Maximum output current		I_{OM}	–	±10	mA
Maximum supply current		I_{SS}, I_{DD}	–	±50	mA
Total power dissipation		P_{tot}	–	500	mW
Storage temperature range		T_{stg}	–55	+150	°C
Operating ambient temperature range		T_{amb}	–40	+70	°C

Note

1. Input voltage should not exceed 7 V.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see “Handling MOS Devices”).

DC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = –40 to +70 °C, unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply						
Supply current	note 1	I_{DD}	–	–	250	µA
	note 2	I_{DD}	–	10	–	mA
Inputs						
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Input voltage LOW		V_{IL}	0	–	0.3 V_{DD}	V
Input current	$V_{SS} \leq V_I \leq$					
	$\leq V_{DD}$	$\pm I_I$	–	–	1	µA
Input capacitance		C_I	–	4	6	pF
Outputs						
OSCL						
Output voltage HIGH	$-I_{OH}$ = 8 mA	V_{OH}	V_{DD}–0.5	–	–	V
Output voltage LOW	I_{OL} = 8 mA	V_{OL}	–	–	0.4	V
OCDB, OLOC, OREF, OPHA,						
OPRE, OSCU, OSDU, OSDA						
Output voltage HIGH	$-I_{OH}$ = 2 mA	V_{OH}	V_{DD}–0.5	–	–	V
Output voltage LOW	I_{OL} = 2 mA	V_{OL}	–	–	0.4	V
OBSY, OWSY, ODCL, OOSC						
Output voltage HIGH	$-I_{OH}$ = 1.5 mA	V_{OH}	V_{DD}–0.5	–	–	V
Output voltage LOW	I_{OL} = 1.5 mA	V_{OL}	–	–	0.4	V
OSDA, ODCL, OWSY, OBSY						
Output leakage current	3-state	$\lvert I_{LO} \rvert$	–	–	15	µA

Notes to the DC characteristics

1. All inputs at V_{DD} or V_{SS}, except ITEST2 on V_{SS}, all outputs open circuit.
2. f_{OSCL} = 11.3 MHz.

AC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V.
T_{amb} = −40 to +70 °C.
Load capacitance (C_L): OSCL = 50 pF; OWSY, ODCL and OSDA = 30 pF (see application note); all other outputs = 20 pF.
Clock frequency f_{IOSCL} = ≤ 12.5 MHz.
IOSCL timing pulse LOW, t_{LOW} ≥ 37 ns; rise and fall times t_r and t_f = ≤ 10 ns.
Delay times are specified from clock input = 50% V_{DD} to output = 50% V_{DD}; unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Set-up and hold times						
IWSEL to IDACL	see Fig.5					
Data set-up time		t_{SU}	1	–	–	note 1
Data hold time		t_{HD}	–	–	1	note 1
Propagation delays						
IOSCL to OSCL		t_p	–	–	25	ns
IDACL to OSDA		t_p	–	–	60	ns
OSCL to OWSY and ODCL		t_p	5	–	50	ns
Rise and fall times						
OSCL						
Rise and fall time	TTL levels = 0.4 to 2 V	t_r, t_f	–	–	10	ns
Rise and fall time	CMOS levels = 10 to 90% V_{DD}	t_r, t_f	–	–	15	ns
OWSY and ODCL						
Rise and fall time	TTL levels = 0.4 to 2 V	t_r, t_f	–	–	15	ns
Rise and fall time	CMOS levels = 10 to 90% V_{DD}	t_r, t_f	–	–	25	ns

Note

1. Clock periods of OSCL.

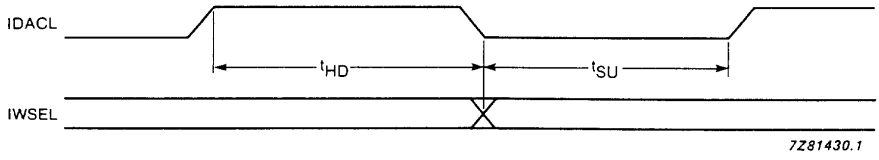
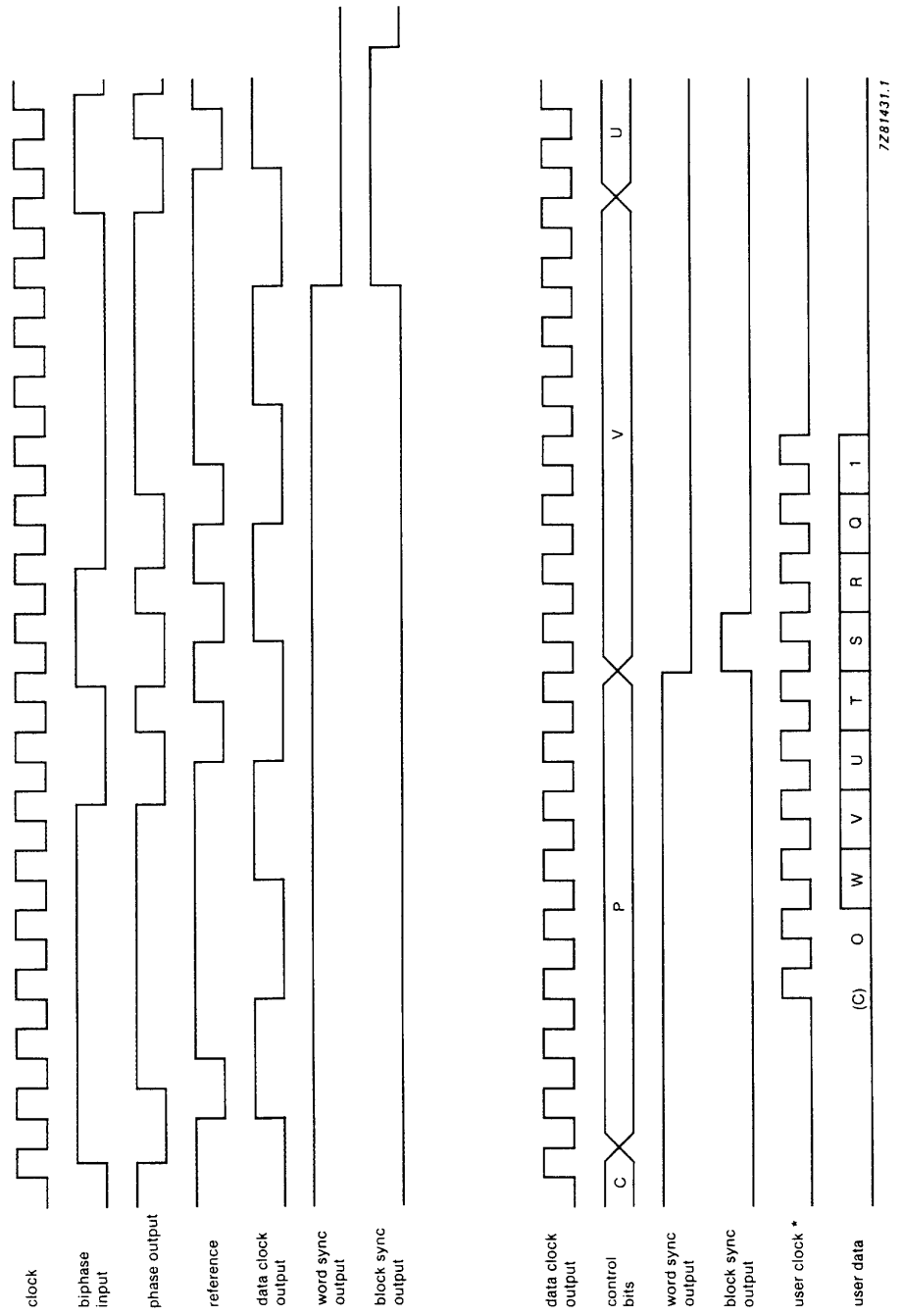


Fig.5 Set-up and hold time diagram.

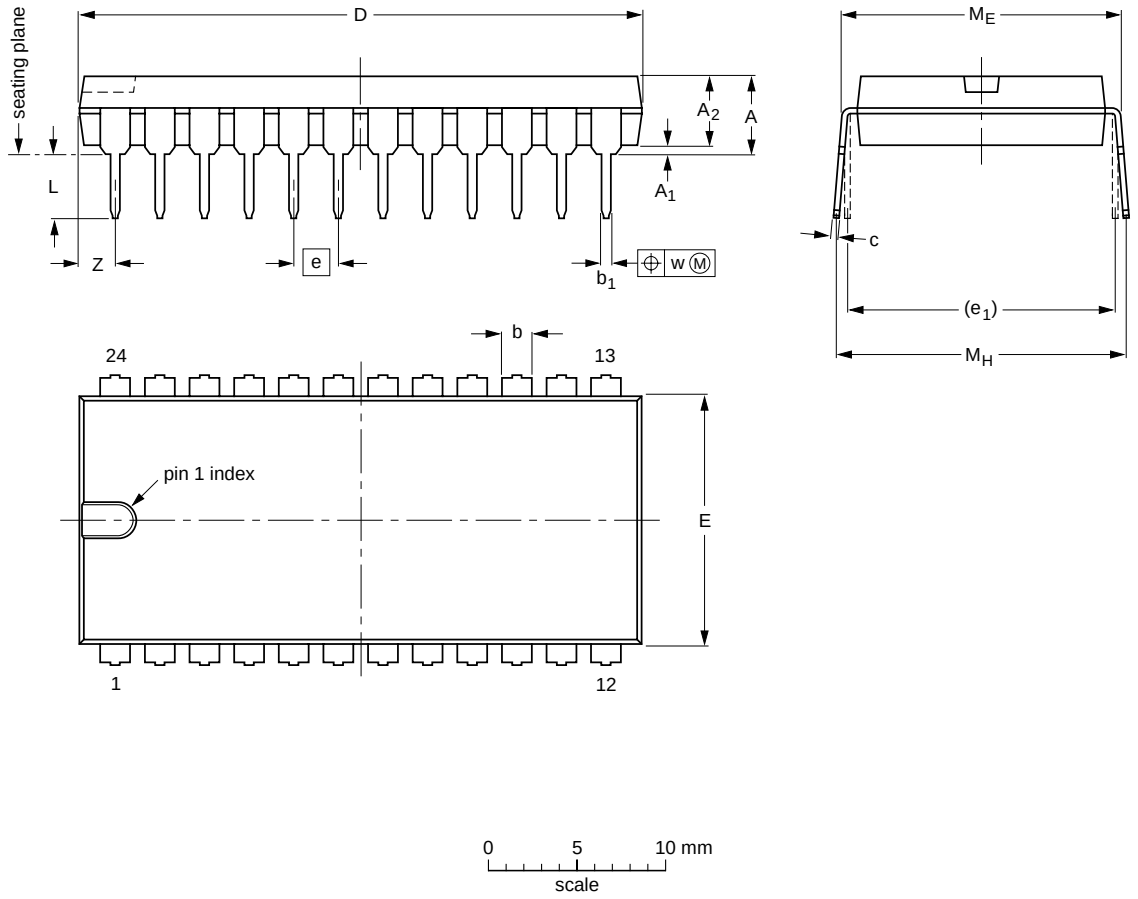


* user clock pattern is not necessarily synchronous with the block sync signal.

Fig.6 Timing diagram.

PACKAGE OUTLINES

DIP24: plastic dual in-line package; 24 leads (600 mil) **SOT101-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

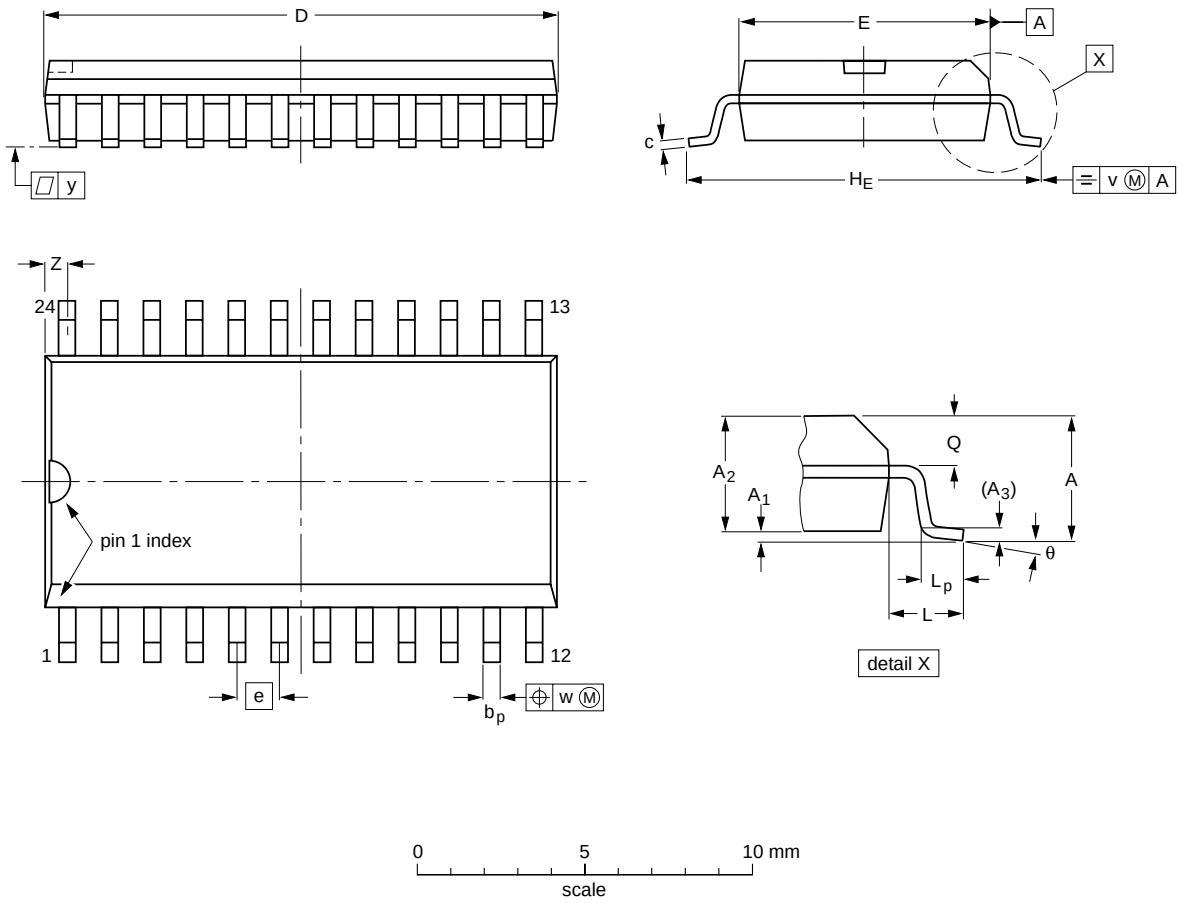
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT101-1	051G02	MO-015AD				~~92-11-17~~ 95-01-23

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.